Ohm Patel

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Education

North Carolina State University — Raleigh, NC
Master of Science in Computer Engineering — *Aug. 2026 – May 2028*
- **Relevant Coursework:** Microprocessor Architecture, ASIC/FPGA Design

North Carolina State University — Raleigh, NC
Bachelor of Science in Computer Engineering – 4.0 GPA; Dean's List — *Aug. 2023 – May 2027*
- **Relevant Coursework:** Microelectronics, Circuits I/II, Digital Systems Design, Computer Architecture, Embedded Systems, Signals & Systems, Data Structures & Algorithms
- **Activities:** IEEE Board Member; IEEE-Eta Kappa Nu Honor Society (Beta Eta Chapter)

Skills

Silicon & Digital: Pre/Post-Silicon Validation, RTL Debug, Digital Logic, Power Management, Verilog, SystemVerilog, FPGA
Hardware & Embedded: C, C++, ARM MCUs, PCB Design, Power Electronics, Motor Control, Firmware, PWM, ADC, FOC
Test & Debug: JTAG, SWD, Oscilloscope, Logic Analyzer, Hardware Tracing, Register-Level Debug, Board Bring-Up
Automation & Tools: Python, Git, GitHub Actions, AI assisted workflows, Synopsys Verdi, Vivado, KiCad, LTspice, Linux

Experience

Silicon Engineering Intern — May 2026 – Present
Intel — *Folsom, CA*
- Validated **pre and post-silicon Intel Nova Lake and next-generation client SoCs**, driving power-management debug across clock/PLL, thermal, reset, low-power, and telemetry subsystems using register-level analysis, RTL simulation, hardware traces, and lab instrumentation
- **Root-caused silicon validation failures across live hardware, RTL, and firmware**; traced hardware behavior in Synopsys Verdi and firmware source to isolate cross-layer defects and deliver actionable fixes to design and firmware owners
- Owned post-silicon telemetry validation spanning **500+ signals, counters, and operating conditions**; developed Python validation tests and triaged failures across silicon, firmware, BIOS, test methodology, and platform configuration
- Built and shipped reusable **silicon-debug and validation automation**, including boot/reset diagnostics that replaced manual register probing and CI/CD infrastructure that automatically synchronizes and validates evolving hardware register collateral
- Engineered **AI-assisted silicon-debug tooling** connecting internal specifications, source code, validation data, and engineering tools to accelerate evidence-driven debug planning and technical research, reducing root-cause investigation time by up to **80%**
- Led organization-wide training on **AI-assisted engineering workflows**, developing tooling, documentation, and best practices for grounded LLM-based silicon debug and validation automation

Undergraduate Researcher — Sep. 2025 – Present
NC State Dept. of Electrical & Computer Engineering – NSF-Funded — *Raleigh, NC*
- Architected embedded firmware for an STM32F407 USB MIDI/CDC controller driving six independent DRSSTC Tesla coils over fiber optic links, implementing deterministic pulse generation, per-channel duty-cycle protection, and watchdog safety systems
- Designed a **4-layer EMI-hardened PCB** integrating fiber-optic drivers, analog emergency-stop circuitry, TVS protection, and power decoupling; performed hardware bring-up and validation using JTAG/SWD and oscilloscope measurements in a high-dV/dt environment
- Developed hardware and augmented-reality visualization platforms supporting NSF-funded electromagnetic and high-voltage engineering education research

Projects

Renesas 4-Channel BLDC Motor Controller | *Senior Design Capstone, RA8T1, Power Electronics, KiCad* — Aug. 2026 – Present
- Designing a **single-MCU four-channel motor-control platform** around the Renesas RA8T1 ARM MCU to concurrently control four BLDC drone motors, replacing traditional one-controller-per-motor architectures with a compact integrated system
- Leading PCB and power-electronics development for four three-phase inverter stages integrating Renesas gate drivers, power MOSFETs, current sensing, gate-drive circuitry, and high-current power distribution
- Defining hardware interfaces and system architecture supporting **FOC, SVPWM, closed-loop motor control, DSHOT command input, and DSHOT/CAN telemetry**, with emphasis on multi-channel power-stage layout and reliable real-time operation

Autonomous Embedded Vehicle | *C, TI MSP430, PWM, ADC, PID, SPI, UART* — Aug. 2025 – Dec. 2025
- Developed register-level embedded firmware for autonomous navigation using IR sensing, ADC acquisition, H-bridge motor control, PWM, timers, interrupts, SPI, and UART on a TI MSP430
- Implemented closed-loop line-following and motion control with PID feedback; built modular peripheral drivers and debugged hardware/firmware interactions using an oscilloscope and logic analyzer

FPGA Digital Systems Design | *Verilog, Vivado, RTL, FSMs, Datapath Design* — Aug. 2025 – Dec. 2025
- Designed and verified synthesizable RTL for arithmetic and sequential systems including an 8×8 Wallace-tree multiplier, carry-select/parallel-prefix arithmetic, and controller/datapath architectures
- Implemented a serial BCD ALU with structured FSM control, shift registers, arithmetic datapaths, and cycle-accurate simulation/verification in Vivado